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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,492	BEAUCAGE, JEAN	
	Examiner	Art Unit	
	Paul Masur	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 12 is objected to because of the following informalities: the dependent claim depends from itself.** It is believed that the applicant intended this claim to depend from independent claim 1, and thus will be treated in this manner for examination purposes. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 7-13, 15-19, 22, 24-26, 30-32, and 34-38 are rejected under 35 U.S.C. 102(b) as being anticipated by "SLK2701 OC-48/24/12/3 SONET?SDH Multirate Transceiver" (now NPL1, referred to as D1 on the ISR).

4. **As per claim 1,** NPL1 teaches a system for broadcasting multi-channel signals to a receiving station over a two-wire bus, comprising:

an encoder having:

a multiplexer for multiplexing digital data corresponding to the channel signals and producing a data stream [NPL1, pg. 2, block diagram, The transmitter contains 3 multiplexers configured to produce a data stream.];

a framer connected to the multiplexer, for breaking the data stream up into

frames, and for inserting into said frame a header containing at least a predetermined pattern [NPL1, pg. 5, “FRAME_EN”, “Frame sync enable. When this pin is asserted high, the frame synchronization circuit for byte alignment is turned on”, The bytes are aligned according to a predetermined frame arrangement.];

a transceiver with pre-emphasis connected to the framer of the encoder and connectable to the two-wire bus [NPL1, pg. 2, block diagram, pg. 4, "STXDOP", “Transmit differential pairs: high-speed serial outputs”, The transmitter sends the frames on a two wire bus.];

a receiver with de-emphasis, connectable to the two-wire bus, said receiver including:

a decoder connectable to the receiving station, the decoder having a de-framer for reproducing the digital data corresponding to selected ones of the multi-channel signals from the frames, said de-framer being adapted to use a previous frame when an error condition is detected in a current frame [NPL1, pg. 2, block diagram, Frame Sync, The Frame Sync takes output from the demultiplexer in order to break the frames down into data.];

a synchronization circuit using a pattern-oriented phase-locked loop for sampling the incoming data stream using said predetermined pattern, and for regenerating a system clock [NPL1, pg. 9, “clock and data recovery”, The systems has a means to synchronize the incoming data and clock.]; and

a channel selector circuit connected to the de-framer and controlling which ones of the multi-channel signals are reproduced by the de-framer [NPL1, pg. 2, block

diagram, pg. 4, “RXDATA[0-3]”, The selected pin indicates the selected channel on the receiver portion.].

5. **As per claim 7,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the multiplexer has a time division multiplexing function [NPL1, pg. 1, “TXDATAO and RXDATAO are the first bits that are transmitted and received in time, respectively”, The data is sent out in a time based manner.].

6. **As per claim 8,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein said header has less transitions than transitions in the digital data [NPL1, pg. 11, frame synchronization, “When enabled, it detects the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream”, The A1 framing pattern has a lower jitter than A2.].

7. **As per claim 9,** NPL1 teaches the system according to claim 8. NPL1 also teaches wherein the header has a size of 17 bits [NPL1, pg. 11, frame synchronization, “When enabled, it detects the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream”, The A1 framing pattern has a lower jitter than A2, and this would be an obvious design constraint.].

8. **As per claim 10,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the frames comprise a parity bit for data integrity check by the decoder [NPL1, pg. 1, “Supports FEC Data Rate of 2.7 Gbps”, FEC provides a parity bit.].

9. **As per claim 11,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the synchronization circuit comprises a sampling circuit for sampling the frames in at a number of times an incoming data rate [NPL1, pg. 11, frame

synchronization, “Frame detection is enabled when-the FRAME_EN pin is high. When enabled, it detects-the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream”, Incoming data is sampled a number of times specific to its rate.], a test circuit for testing a phase relation of the frames with an internal reference [NPL1, pg 1., “The SLK2701 device provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback”, A test circuit using loopback means there is a phase comparison in the testing process.], and a phase lock loop circuit responsive to the test circuit for phase correction of the synchronization circuit [NPL1, pg. 9, “clock and data recovery”, The systems has a means to synchronize the incoming data and clock.].

10. **As per claim 12,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the test circuit is adapted to perform a phase comparison after finding a predetermined bit pattern in the data stream [NPL1, pg 1., “The SLK2701 device provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback”, A test circuit using loopback means there is a phase comparison in the testing process.].

11. **As per claim 13,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the channel selector circuit comprises a user interface for selection of said ones of the multi-channel signals [NPL1, pg. 1, “Low Jitter PECL-Compatible Differential Serial Interface With Programmable De-Emphasis for the Serial Output”, The outputs are selected via user programming.].

12. **As per claim 15,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the de-framer comprises a synchronization analyzer receiving a signal indicative of the selected ones of the multi-channel signals [NPL1, pg. 9, "clock and data recovery", The systems has a means to synchronize the incoming data and clock.], and serial to parallel converting circuitry controlled by the analyzer for providing the digital data into parallel form [NPL1, pgs. 2 & 5, "P/N", "Receive data pins. Parallel data on this bus is valid on the falling edge of RXCLKP ~refer to Figure 7). RXDATA0 is the first bit received in time", The output data of the receiving side is in parallel and digital form.].

13. **As per claim 16,** NPL1 teaches the system according to claim 1. NPL1 also teaches further comprising a data repeater connectable between the two-wire bus and an additional two-wire bus, for rebuilding, cleaning up and repeating the frames for transmission on the additional two-wire bus [NPL1, pg. 12, remote loopback, pg. 7, "While the transceiver mode, transmit only mode, and receive only mode are straightforward, the repeater mode of operation is shown in Figure 5", The transceiver operates in a repeater mode.].

14. **As per claim 17,** NPL1 teaches the system according to claim 16. NPL1 also teaches wherein:

the data repeater comprises a sampler for sampling the frames in at a number of times an incoming data rate [NPL1, pg. 11, frame synchronization, "Frame detection is enabled when-the FRAME_EN pin is high. When enabled, it detects the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream", Incoming data is sampled a number of times specific to its rate.], a test

circuit for testing a phase relation with an internal reference [NPL1, pg 1., “The SLK2701 device provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback”, A test circuit using loopback means there is a phase comparison in the testing process.], a feedback circuit responsive to the test circuit for correction of the internal reference used by the sampler and the test circuit [NPL1, pg.10, “REFCLK is still needed for the recovery loop operation.”, The REFCLK is used by the test circuit in performing the test.], and a correction circuit for phase correction of the frames going out from the repeater [NPL1, pg. 9, “clock and data recovery”, The systems has a means to synchronize the incoming data and clock.]; and

the system further comprising a transceiver with pre-emphasis connected to the data repeater and connectable to the additional two-wire bus [NPL1, pg. 2, block diagram, pg. 4, "STXDOP", “Transmit differential pairs: high-speed serial outputs”, The transmitter sends the frames on a two wire bus.].

15. **As per claim 18,** NPL1 teaches the system according to claim 17. NPL1 also teaches wherein the data repeater has a phase locked on one clean pulse intentionally generated by the encoder, the frames being sampled by the sampler based on the phase [NPL1, pg. 4, FSYNCP, “Frame sync pulse. This signal indicates the frame boundaries of the incoming data stream. I1 the frame-detect circuit is enabled. FSYNC pulses for four RXCLKP and RXCLKN clock cycles when it detects the framing patterns”, The clean pulse is used for sampling purposes].

16. **As per claim 19,** NPL1 teaches the system according to claim 17. NPL1 also teaches wherein the correction circuit comprises a digital filter [NPL1, pg. 9, minimum

transition density, “The loop filter transfer function is optimized to enable the CDR to track ppm difference in the clocking and tolerate the minimum transition density that can be received in a SONET data signal (+_20 ppm)”, PPM is tracked by a digital filter, since it affects the clock and data recovery function.].

17. **As per claim 22,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the multi-channel signals comprise high speed applications [NPL1, pg. 1, “The SLK2701 device supports an FEC data rate up to 2.7 Gbps when configured to operate at the 0C-48 data rate and provided with an external reference clock that is properly scaled”, Gigabit data rates encompass high speed applications.].

18. **As per claim 24,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the receiver has outputs for connection to the decoder and to additional like decoders [NPL1, pg. 2, block diagram, The demultiplexer is connected to the Frame Sync and the PBRS verification.].

19. **As per claim 25,** NPL1 teaches the system according to claim 1. NPL1 also teaches wherein the two-wire bus forms a serial multi-drop communication network [NPL1, pg. 2, block diagram, pg. 4, "STXDOP", “Transmit differential pairs: high-speed serial outputs”, The transmitter sends the frames on a two wire bus to multiple destinations.].

20. **As per claim 26,** NPL1 teaches a method of broadcasting high-speed applications over a serial multi-drop communication network, comprising:

time-division multiplexing the high-speed applications to produce a data stream [NPL1, pg. 1, “TXDATAO and RXDATAO are the first bits that are transmitted and received in time, respectively”, The data is sent out in a time based manner.];

framing the data stream into frames having a header and a parity bit [NPL1, pg. 2, block diagram, pg. 4, "STXDOP", “Transmit differential pairs: high-speed serial outputs”, The transmitter sends the frames on a two wire bus.], the header having a size lower than 32 bits [NPL1, pg. 1, "TheSLK2701 device is a single chip multirate transceiver that derives high-speed timing signals for SONET/ SDH-based equipment", SONET equipment can handle headers less than 32 bits, i.e. 16 bits.];

transmitting the frames with pre-emphasis over the serial multi-drop communication network [NPL1, pg. 2, block diagram, pg. 4, "STXDOP", “Transmit differential pairs: high-speed serial outputs”, The transmitter sends the frames on a two wire bus.];

receiving the frames with de-emphasis from the serial multi-drop communication network [NPL1, pg. 2, block diagram, Frame Sync, The Frame Sync takes output from the demultiplexer in order to break the frames down into data.];

detecting a predetermined bit pattern in the received frames [NPL1, pg 1., “The SLK2701 device provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback”, A test circuit using loopback means there is a phase comparison in the testing process.];

synchronizing the received frames using an internal clock signal and an external clock signal found within the frames following a phase comparison made after detection

of the predetermined bit pattern [NPL1, pg. 9, “clock and data recovery”, The systems has a means to synchronize the incoming data and clock.]; and

de-framing the synchronized frames into a selected one of the high-speed applications [NPL1, pg. 1, “The SLK2701 device supports an FEC data rate up to 2.7 Gbps when configured to operate at the 0C-48 data rate and provided with an external reference clock that is properly scaled”, Gigabit data rates encompass high speed applications.].

21. **As per claim 30,** NPL1 teaches the method according to claim 26. NPL1 also teaches further comprising parallel to series converting the high-speed applications prior to the multiplexing, and series to parallel converting the selected one of the high-speed applications [NPL1, pg. 1, "The device performs clock and data recovery, serial-to-parallel/parallel-to-serial conversion, and a frame detection function conforming to the SONET/SDH standard", The device performs these operations in a high speed environment.].

22. **As per claim 31,** NPL1 teaches the method according to claim 26. NPL1 also teaches further comprising checking data integrity of the synchronized frames using the parity bit [NPL1, pg. 1, “Supports FEC Data Rate of 2.7 Gbps”, FEC provides a parity bit.].

23. **As per claim 32,** NPL1 teaches the method according to claim 31. NPL1 also teaches wherein a previously received frame is used when an error condition is detected in a currently received frame [NPL1, pg. 1, “Supports FEC Data Rate of 2.7 Gbps”, FEC provides a parity bit.].

24. **As per claim 34,** NPL1 teaches the method according to claim 26. NPL1 also teaches wherein the predetermined bit pattern is located in the header of the frames [NPL1, pg. 11, frame synchronization, “When enabled, it detects the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream”, The A1 framing pattern has a lower jitter than A2.].

25. **As per claim 35,** NPL1 teaches the method according to claim 26. NPL1 also teaches further comprising compressing the high-speed applications prior to the framing, and decompressing the selected one of the high-speed applications after the de-framing [NPL1, pg. 1, "The device performs clock and data recovery, serial-to-parallel/parallel-to-serial conversion, and a frame detection function conforming to the SONET/SDH standard", The device performs these operations in a high speed environment.].

26. **As per claim 36,** NPL1 teaches the method according to claim 26. NPL1 also teaches further comprising repeating the frames for transmission over another segment of the serial multi-drop communication network [NPL1, pg. 12, remote loopback, pg. 7, “While the transceiver mode, transmit only mode, and receive only mode are straightforward, the repeater mode of operation is shown in Figure 5”, The transceiver operates in a repeater mode.].

27. **As per claim 37,** NPL1 teaches the method according to claim 26. NPL1 also teaches wherein the repeating comprises sampling the frames in at a number of times an incoming data rate [NPL1, pg. 11, frame synchronization, “Frame detection is enabled when-the FRAME_EN pin is high. When enabled, it detects the A1, A2 framing

pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream", Incoming data is sampled a number of times specific to its rate.], testing a phase relation with an internal reference [NPL1, pg 1., "The SLK2701 device provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback", A test circuit using loopback means there is a phase comparison in the testing process.], phase correcting the frames going out to the other segment [NPL1, pg. 9, "clock and data recovery", The systems has a means to synchronize the incoming data and clock.], and transmitting the frames with pre-emphasis to the other segment [NPL1, pg. 2, block diagram, pg. 4, "STXDOP", "Transmit differential pairs: high-speed serial outputs", The transmitter sends the frames on a two wire bus.].

28. **As per claim 38,** NPL1 teaches the method according to claim 37. NPL1 also teaches further comprising inserting a clean pulse in the frames, and locking a phase on the clean pulse for sampling the frames [NPL1, pg. 4, FSYNCP, "Frame sync pulse. This signal indicates the frame boundaries of the incoming data stream. I1 the frame-detect circuit is enabled. FSYNC pulses for four RXCLKP and RXCLKN clock cycles when it detects the framing patterns", The clean pulse is used for sampling purposes.].

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 2-4, 14, 20, 23, 27, 28, and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over "SLK2701 OC-48/24/12/3 SONET?SDH Multirate Transceiver" (now NPL1, referred to as D1 on the ISR) in view of Huang (US Patent No. 6,646,581).

31. **As per claim 2,** NPL1 teaches the system according to claim 1. NPL1 does not teach wherein: the encoder has delta-sigma analog-to-digital converters for converting the multi-channel signals into digital form for the multiplexer; and the decoder has a delta-sigma digital-to-analog converter connected to the de-framer for converting the digital data corresponding to the selected ones of the multi-channel signals into analog form for the receiving station.

However, Huang teaches the encoder has delta-sigma analog-to-digital converters for converting the multi-channel signals into digital form for the multiplexer [Huang, column 10, lines 32-35, "sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values", The DAC can be configured to encode in order to assist the multiplexer.]; and

the decoder has a delta-sigma digital-to-analog converter connected to the de-framer for converting the digital data corresponding to the selected ones of the multi-channel signals into analog form for the receiving station [Huang, column 10, lines 32-35, "sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values", The DAC can be configured to decode in order to assist the demultiplexer.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

32. **As per claim 3,** The system according to claim 2. NPL1 does not teach wherein the encoder comprises analog interfaces respectively having amplifiers in series with low pass filters for amplifying and filtering the multi-channel signals transmitted to the delta-sigma analog-to-digital converters.

However, Huang teaches wherein the encoder comprises analog interfaces respectively having amplifiers in series with low pass filters for amplifying and filtering the multi-channel signals transmitted to the delta-sigma analog-to-digital converters [Huang, fig. 2, elements 123, & 126, column 4, lines 3-7, "control signal generator circuit 126 which receives the output signal 130 from the loop filter 123. Exemplary voltage levels for each control signal 122 are shown in FIG. 4 for up to N+1 control signals 122. As shown in FIG. 4, the voltage levels for a given control signal 122 may range from a low voltage reference level VREFL to a high voltage reference level VREFH and each control signal 122 is offset slightly from the adjacent control signals 122 for a given value of the input signal to the control signal generator circuit 126", The encoder has a variety of filters and amplifiers to improve the multi channel signals as they endure DAC.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

33. **As per claim 4,** NPL1 teaches the system according to claim 1. NPL1 does not teach wherein: the encoder comprises a compression circuit for compressing the digital data input into the framer; and the decoder comprises a decompression circuit for decompressing the digital data output by the de-framer.

However, Huang teaches the encoder comprises a compression circuit for compressing the digital data input into the framer [Huang, column 10, lines 32-35, "sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values", The DAC can be configured to encode in order to assist the multiplexer.; and

the decoder comprises a decompression circuit for decompressing the digital data output by the de-framer [Huang, column 10, lines 32-35, "sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values", The DAC can be configured to decode in order to assist the demultiplexer.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of

analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

34. **As per claim 14,** NPL1 teaches the system according to claim 1. NPL1 also teaches a user interface for adjusting a gain of the variable gain amplifier [NPL1, pg. 1, "Low Jitter PECL-Compatible Differential Serial Interface With Programmable De-Emphasis for the Serial Output", The outputs are selected via user programming.]. NPL1 does not teach wherein the decoder has a variable gain amplifier for amplifying the selected ones of the multi-channel signals.

However, Huang teaches wherein the decoder has a variable gain amplifier for amplifying the selected ones of the multi-channel signals [Huang, fig. 2, elements 123, & 126, column 4, lines 3-7, "control signal generator circuit 126 which receives the output signal 130 from the loop filter 123. Exemplary voltage levels for each control signal 122 are shown in FIG. 4 for up to N+1 control signals 122. As shown in FIG. 4, the voltage levels for a given control signal 122 may range from a low voltage reference level VREFL to a high voltage reference level VREFH and each control signal 122 is offset slightly from the adjacent control signals 122 for a given value of the input signal to the control signal generator circuit 126", The encoder has a variety of filters and amplifiers to improve the multi channel signals as they endure DAC.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of

analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

35. **As per claim 20,** NPL1 teaches the system according to claim 17. NPL1 does not teach wherein the number of times is higher than a number of times the frames are sampled by the decoder.

However, Huang teaches wherein the number of times is higher than a number of times the frames are sampled by the decoder [Huang, column 22, lines 1-4, "a second order sigma-delta modulator can have a lower over-sampling ratio and still achieve the same signal-to-noise ratio (e.g., quantization noise) as a first-order sigma-delta modulator", The closed loop operating DAC performs oversampling.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

36. **As per claim 23,** NPL1 in view of Huang teaches the system according to claim 2,. NPL1 does not teach wherein the decoder has at least one additional delta-sigma digital-to-analog converter connected to the de-framer, for converting the digital data corresponding to additional selected ones of the multi-channel signals.

However, Huang teaches wherein the decoder has at least one additional delta-sigma digital-to-analog converter connected to the de-framer, for converting the digital data corresponding to additional selected ones of the multi-channel signals [Huang,

column 10, lines 32-35, “sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values”, The DAC can be configured to decode in order to assist the demultiplexer.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

37. **As per claim 27,** NPL1 teaches the method according to claim 26. NPL1 does not teach further comprising analog-to-digital converting the high-speed applications prior to the multiplexing, and digital-to-analog converting the selected one of the high-speed applications after the de-framing.

However, Huang teaches further comprising analog-to-digital converting the high-speed applications prior to the multiplexing [Huang, column 10, lines 32-35, “sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values”, The DAC can be configured to encode in order to assist the multiplexer.], and digital-to-analog converting the selected one of the high-speed applications after the de-framing [Huang, column 10, lines 32-35, “sigma-delta modulators may also be implemented to encode additional bits of significance into a smaller number of bits, at least when averaged over multiple values”, The DAC can be configured to decode in order to assist the demultiplexer.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

38. **As per claim 28,** NPL1 in view of Huang teaches the method according to claim 27. NPL1 does not teach wherein the analog-to-digital converting and the digital-to-analog converting comprise over sampling and closed-loop modulating the high-speed applications.

However, Huang teaches wherein the analog-to-digital converting and the digital-to-analog converting comprise over sampling and closed-loop modulating the high-speed applications [Huang, column 22, lines 1-4, “a second order sigma-delta modulator can have a lower over-sampling ratio and still achieve the same signal-to-noise ratio (e.g., quantization noise) as a first-order sigma-delta modulator”, The closed loop operating DAC performs oversampling.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

39. **As per claim 39,** NPL1 teaches the method according to claim 37. NPL1 does not teach wherein the number of times is higher than a number of times the frames are sampled in the synchronizing.

However, Huang teaches wherein the number of times is higher than a number of times the frames are sampled in the synchronizing [Huang, column 22, lines 1-4, "a second order sigma-delta modulator can have a lower over-sampling ratio and still achieve the same signal-to-noise ratio (e.g., quantization noise) as a first-order sigma-delta modulator", The closed loop operating DAC performs oversampling.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Huang into NPL1, since NPL1 suggests a transceiver for SONET networks, and Huang suggests the beneficial use of analog to digital encoders and decoders such as to operate in a SONET network [column 25, line 25] in the analogous art of SONET.

40. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over "SLK2701 OC-48/24/12/3 SONET?SDH Multirate Transceiver" (now NPL1, referred to as D1 on the ISR) in view of Short et al. (WO 03/084121, referred to as D3 on the ISR).

41. **As per claim 5,** NPL1 in view of Huang teaches the system according to claim 4. NPL1 does not teach wherein the compression circuit and the decompression circuit have look-up tables defining compression and decompression functions respectively.

However, Short et al. teaches wherein the compression circuit and the decompression circuit have look-up tables defining compression and decompression

functions respectively [Short, pg. 12, lines 21-22, "Data is compressed by using the look-up table", Data is compressed using a look-up table.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Short et al. into NPL1, since NPL1 suggests a transceiver for SONET networks, and Short et al. suggests the beneficial use of compression and decompression of data such as to achieve high data speeds [Short, pg. 12, lines 21-22] in the analogous art of high speed data networks.

42. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over "SLK2701 OC-48/24/12/3 SONET?SDH Multirate Transceiver" (now NPL1, referred to as D1 in ISR) in view of Suzuki et al. (EP 1,215,848, referred to as D4 on the ISR).

43. **As per claim 6,** NPL1 in view of Huang teaches the system according to claim 4. NPL1 does not teach wherein the compression circuit and the decompression circuit respectively have logarithmic and antilogarithmic functions.

However, Suzuki et al. teaches wherein the compression circuit and the decompression circuit respectively have logarithmic and antilogarithmic functions [Suzuki, paragraph 0020, "As to the quantization and the like, the encoder circuit 13 employs an 8-bit logarithmic quantization scheme which compresses a sampled signal in conformity to an A-law or a i- low which is generally used for PCM communication lines. A decoder circuit 14 is a circuit for decoding a PCM signal received from another Bluetooth device existing in the same piconet by decompressing the PCM signal in

accordance with the reverse characteristic of the encoder circuit 13", Logarithmic and anti-logarithmic functions are used by a decoder and encoder.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Suzuki et al. into NPL1, since NPL1 suggests a transceiver for SONET networks, and Suzuki et al. suggests the beneficial use of logarithmic based compression such as to quantize digital data [Suzuki, paragraph 0020] in the analogous art of digital data networks.

44. Claims 21 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over "SLK2701 OC-48/24/12/3 SONET?SDH Multirate Transceiver" (now NPL1, referred to as D1 on the ISR) in view of LaDue (US PG Pub 2005/0147057).

45. **As per claim 21,** NPL1 teaches the system according to claim 1. NPL1 does not teach wherein the high-speed applications comprise a multi-channel audio signal broadcast to audio listening stations connected to the serial multi-drop communication network.

However, LaDue teaches wherein the high-speed applications comprise a multi-channel audio signal broadcast to audio listening stations connected to the serial multi-drop communication network [LaDue, paragraph 0050, "The search for improved record, storage and playback resolution has always been the central aim and goal of all audio reproducing equipment manufactures such as electronic musical instruments made by Roland, stereo manufactures such as Marantz, and digital mobile phone manufactures such as Nokia. Musicians, music listeners and digital mobile phone users all want good audio quality from their digital devices"].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of LaDue into NPL1, since NPL1 suggests a transceiver for SONET networks, and LaDue suggests the beneficial use of improved audio equipment such as to run on a SONET [LaDue, paragraph 0065] in the analogous art of SONET.

46. **As per claim 33,** NPL1 teaches the method according to claim 26. NPL1 does not teach wherein the high-speed applications comprise a multi-channel audio signal broadcast to audio listening stations connected to the serial multi-drop communication network.

However, LaDue teaches wherein the high-speed applications comprise a multi-channel audio signal broadcast to audio listening stations connected to the serial multi-drop communication network [LaDue, paragraph 0050, "The search for improved record, storage and playback resolution has always been the central aim and goal of all audio reproducing equipment manufactures such as electronic musical instruments made by Roland, stereo manufactures such as Marantz, and digital mobile phone manufactures such as Nokia. Musicians, music listeners and digital mobile phone users all want good audio quality from their digital devices"].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of LaDue into NPL1, since NPL1 suggests a transceiver for SONET networks, and LaDue suggests the beneficial use of improved audio equipment such as to run on a SONET [LaDue, paragraph 0065] in the analogous art of SONET.

47. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over "SLK2701 OC-48/24/12/3 SONET?SDH Multirate Transceiver" (now NPL1, referred to as D1 in ISR) in view of Ahmed et al. (US PG Pub 2005/0114903).

48. **As per claim 29,** NPL1 teaches the method according to claim 26. NPL1 does not teach wherein the high-speed applications comprise a multi-channel signal broadcast.

However, Ahmed et al. teaches wherein the high-speed applications comprise a multi-channel signal broadcast [Ahmed, abstract, "Downstream analog and digital video channels in the digital format are transmitted using time-division multiplex technology from a headend to nodes using standard network protocols, such as SONET...The digital node transmitter also frequency-division multiplexes multiple analog or digital video channels into one analog broadband signal for broadcast to subscribers' homes", The node transmitter can broadcast signals within SONET.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Ahmed et al into NPL1, since NPL1 suggests a transceiver for SONET networks, and Ahmed et al. suggests the beneficial use of a node transmitter such as to achieve a multi-channel broadcast [Ahmed, abstract] in the analogous art of SONET.

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The reference Hill et al. (US PG Pub 2004/0034581) teaches a two-wire bus network in accordance with RS-485 architecture.

The reference Karolys et al. (US PG Pub 2002/0012401) teaches a two-wire bus system that uses TDM for digital data with RS-485 clock signals.

50. **Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Masur whose telephone number is (571) 270-7297.** The examiner can normally be reached on Monday through Friday from 7:00AM to 4:30PM (Eastern Time).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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